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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/017,793	12/12/2001	Youfeng Wu	042390.P12589	9134

7590 01/03/2006

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EXAMINER	
TREAT, WILLIAM M	
ART UNIT	**PAPER NUMBER**
2181	

DATE MAILED: 01/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/017,793	WU ET AL.	
	Examiner	Art Unit	
	William M. Treat	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,13-24 and 27* is/are rejected.

7)☒ Claim(s) *12,25 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-27 are presented for examination.

2. In view of the appeal brief filed on 10/17/2005, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

3. To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

4. A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below.

5. The drawings are objected to because (1) the drawings lack suitable legends, 37 CFR 1.84(o), (only abbreviations and initials instead of descriptive words), different reference characters seem to designate the same element, 37 CFR 184(p), (100, 172, 170), reference characters seem to float in a void (175), and reference characters in the specification are not found in the drawings (174). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if

only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

6. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the second processor of claims 5 and 15 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

7. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate

changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claim 15 recites the limitation "the first processor" in lines 2-3. There is an antecedent basis problem related to this limitation in the claim. If there is a first processor, this implies the presence of a second processor. However, applicants' drawings and specification do not seem to support the presence of a second processor when both pipelines are encompassed by the first processor.

10. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

11. The claimed invention of claims 20-23 is directed to non-statutory subject matter. Applicants appear to have defined their computer-readable medium to encompass electromagnetic signals (p. 11, lines 4-11 of applicants' specification). As stated in the Office's "Interim Guidelines for Examination of Patent Applications for Patent Subject Matter Eligibility", "it does not appear that a claim reciting a signal encoded with

functional descriptive material falls within any of the categories of patentable subject matter set forth in 101". The Office's "Interim Guidelines for Examination of Patent Applications for Patent Subject Matter Eligibility" were released on October 26th. See pages 55-57 of the interim guidelines. The website is:

http://www.uspto.gov/web/offices/pac/dapp/opla/preognotice/guidelines101_20051026.pdf

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

13. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Sundaramoorthy et al. (Multipath Execution...)

14. Sundaramoorthy taught the invention of exemplary claim 1 including including a data processing apparatus (Figure 1), comprising: a first pipeline (Section 2, first sentence) having a data cache (L1 D-cache) and an instruction cache (L1 I-cache); a second pipeline (Section 2, first sentence) coupled to the data cache (L1 D-cache) and the instruction cache (L1 I-cache); and a data value prediction module (CQ, value predictions) coupled to the second pipeline (Figure 1).

15. As to claim 2, Sundaramoorthy taught the data processing apparatus of claim 1, further comprising: a first instruction fetch module coupled to the first pipeline; and a second instruction fetch module coupled to the second pipeline (Section 1, 4th paragraph, where it teaches both pipelines fetch instructions and, therefore, would inherently have fetch modules).

16. As to claim 3, Sundaramoorthy taught the data processing apparatus of claim 2, further comprising: a branch predictor coupled to the first and second instruction fetch modules (Figure 1 and Section 1, 5th paragraph, where it teaches the PEs follow opposite paths of the branch prediction meaning, inherently, both fetch modules must be connected to a branch predictor to know which path to fetch). Applicants claim language does not require both fetch modules be connected to a single branch predictor.

17. Claims 1, 4-8, 10, 13-16, 19-20, and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Rotenberg et al. (Trace Processors).

18. Rotenberg taught the invention of claim 1 including a data processing apparatus (Figure 1), comprising: a first pipeline (Processing Elements 0, 1, 2, 3 and Section 1.1, last paragraph) having a data cache (Section 2.4.2) and an instruction cache (Figures 1 and 2); a second pipeline (Processing Elements 0, 1, 2, 3 and Section 1.1, last paragraph) coupled to the data cache (section 2.4.2) and the instruction cache (Figures 1 and 2); and a data value prediction module (Section 2.2) coupled to the second pipeline (Processing Elements 0, 1, 2, 3, Live-in Value Predictor, and Section 1.1, last paragraph).

19. As to claim 4, Rotenberg taught the data processing apparatus of claim 1, further comprising: a first register file coupled to the first pipeline; and a second register file coupled to the second pipeline (Processing Elements 0, 1, 2, 3 and Section 1.1, last paragraph).

20. As to claim 5, Rotenberg taught the data processing apparatus of claim 1, wherein the first pipeline is included in a first processor, and wherein the second pipeline is included in a second processor (Processing Elements 0, 1, 2, 3 and Section 1.1, last paragraph – The result is a processor **composed of processing elements (PE), each having the organization of a small-scale superscalar processor**).

21. As to claim 6, Rotenberg taught the data processing apparatus of claim 1, wherein the first and second pipelines are included in a single processor (Processing Elements 0, 1, 2, 3 and Section 1.1, last paragraph – The result is a **processor** composed of processing elements (PE), each having the organization of a small-scale superscalar processor).

22. As Rotenberg describes his Trace Processor, it is a processor composed of small-scale superscalar processors which meets the limitations of the language of applicants' claims 5 and 6. Were applicants to try to refine their language further in relation to what is a processor and what isn't, it is unlikely such language would distinguish over the Rotenberg in view of what one of ordinary skill knows of fabrication of multiple components and processors upon one or more chips.

23. As to claim 7, Rotenberg taught the data processing apparatus of claim 6, wherein the data cache, the instruction cache, and the data value prediction module are included in the single processor (Figure 1 entitled "A Trace Processor").

24. As to claim 8, Rotenberg taught the data processing apparatus of claim 1, further comprising: a value prediction table coupled to the value prediction module (Section 2.2).

25. As to claim 10, Rotenberg taught the data processing apparatus of claim 1, further comprising: a storage buffer coupled to the second pipeline (Section 2.3).

26. As to claim 13-14, 16, and 19, they fail to teach or define over rejected claims 1, 4-8, and 10.

27. As to claim 15, Rotenberg taught the computer of claim 13, further comprising: a bus coupled to the data cache and the memory, wherein the first processor included the second pipeline (Processing Elements 0, 1, 2, 3 and Section 1.1, last paragraph – The result is a **processor** composed of processing elements (PE), each having the organization of a small-scale superscalar processor). In this instance the trace processor and computer are one and the same. This interpretation is not precluded by applicants' claim language and seems consistent with applicants' drawings.

28. As to claim 24, Rotenberg taught the method of claim 24, comprising: executing a plurality of instructions including a LOAD instruction using a first pipeline sharing an instruction cache and a data cache with a second pipeline; calculating a predicted load value for execution of the LOAD instructions if a cache miss in the data cache results when the second pipeline executes the LOAD instruction before the first pipeline; and continuing execution of the plurality of instructions using the second pipeline (Sections 2.4, 2.4.1, 2.4.2).

29. As to claim 20, it fails to teach or define over rejected claims 1, and 4-8, 10, 13-16, 19, and 24.

30. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

31. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

32. Claims 9, 11, 17, 18, 23, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rotenberg et al. (Trace Processors) in view of Rotenberg (AR-SMT: A Microarchitectural Approach...).

33. Rotenberg (Trace...) taught the invention of independent claims 1, 13, 20, and 24 from which claims 9, 11, 17, 18, 23, and 27 depend.

34. As to claim 9, Rotenberg et al. (Trace Processors) did not teach the data processing apparatus of claim 1, further comprising: a main memory coupled to the data cache, wherein the first pipeline may operate to store a data value to the main memory, and wherein the second pipeline may not operate to store the data value to the main memory. However, Rotenberg (AR-SMT: A Microarchitectural Approach...) taught one of ordinary skill in the art knew the trace processor architecture of Rotenberg et al. (Trace Processors) could be advantageously applied to advance-stream/redundant-

stream processing (Section 1.3.2 and item 17 of References) and that the first pipeline may operate to store a data value to the main memory, and the second pipeline may not operate to store the data value to the main memory. Inherently, with a trace processor with advance and redundant threads there will be mispredictions as to instruction path. Stores done by the advance processor may not be replicated by the redundant processor when such mispredictions are uncovered.

35. As to claim 11, Rotenberg (AR-SMT: A Microarchitectural Approach...) taught the data processing apparatus of claim 1, further comprising: a synchronization mechanism coupled to the second pipeline (Section 2.2.2). As to a reason for combination for the teachings of Rotenberg (AR-SMT: A Microarchitectural Approach...) with the teachings of Rotenberg et al. (Trace Processors), see paragraph 34, *supra*.

36. As to claim 17, it fails to teach or define over rejected claims 1-11, 13-16, 19-20, and 24.

37. As to claim 18, Rotenberg (AR-SMT: A Microarchitectural Approach...) taught the advance pipeline can only run ahead of the redundant pipeline by an amount equal to the length of the Delay Buffer (Section 2.1.4, 6th paragraph) and that the Delay Buffer is essentially a FIFO queue where the results of each instruction committed by the advance pipeline are pushed onto the queue (Section 1.2, 1st paragraph). A conventional means of assuring that values of such a FIFO would not be overwritten (i.e., the advance pipeline would remain synchronized with the redundant pipeline and would not run too far ahead and overwrite results before the redundant pipeline read them) would be to use a counter which incremented when results of an instruction were

written to the Delay Buffer and decremented when results were read from the Delay Buffer. One of ordinary skill would be motivated to use such a runahead counter because it is a conventional means which is reliable and readily implemented. As to a reason for combination for the teachings of Rotenberg (AR-SMT: A Microarchitectural Approach...) with the teachings of Rotenberg et al. (Trace Processors), see paragraph 34, *supra*.

38. As to claim 27, Rotenberg (AR-SMT: A Microarchitectural Approach...) taught the method of claim 24, further comprising: beginning execution of the plurality of instructions by the first and second pipelines at a same program counter value (Section 2.2.2, 1st three sentences, where it is described that the advanced and redundant pipelines are synchronized at a point where their two contexts are identical – i.e., their program counters contain the same value). As to a reason for combination for the teachings of Rotenberg (AR-SMT: A Microarchitectural Approach...) with the teachings of Rotenberg et al. (Trace Processors), see paragraph 34, *supra*.

39. As to claim 23, it fails to teach or define over rejected claims 1-11, 13-20, 24, and 27.

40. Claims 12, 25 and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

41. Any inquiry concerning this communication should be directed to William M. Treat at telephone number 703 305 9699. After Oct. 12, 2004, the examiner's phone number should be changed to (571) 272-4175. The examiner works at home on

Wednesdays but may normally be reached on Wednesdays by leaving a voice message using his office phone number. The examiner also works a flexible schedule but may normally be reached in the afternoon and evening on three of the four remaining weekdays.

42. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WILLIAM M. TREAT
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